



Olympus Integrated Technologies America takes on IR Inspection and Metrology of Bonded Wafers



Over the past 2 years, Olympus has been working alongside SEMATECH researchers to develop 3D metrology methodologies and automated tools based on infrared (IR) microscopy to perform inspection on bonded wafer pairs. Olympus uses IR metrology because of the lack of transparency of silicon. At SEMICON West 2011, Chip Scale Review caught up with Greg Baker, president and COO for an update on the projects' progress.

CSR: What was the initial purpose of this joint development program between Olympus and SEMATECH?

GB: Inspection of bonded wafers is one of the identified hurdles for market adoption of 3D integration with TSVs. We entered into this JDP with the goal of adapting one of our core technologies, an IR laser scanning confocal microscope, to bonded wafer and bonded die metrology and defect inspection. The intention was to take the IR confocal microscope and integrate it into a fully automated overlay metrology and defect inspection system. In achieving this, we needed to meet four major goals.

The first goal was to develop automated overlay alignment measurement. This involved being able to automatically focus on the very narrow bonded interface between wafers and acquire a high resolution image with which we could accurately and repeatably measure alignment offset. Second was to develop automated thickness measurements. This is where the confocal capability of the microscope comes into play so that we can create accurate three dimensional reconstructions and cross sections of the wafers and bonded interface for measurement. The third goal was to develop defect review capabilities to review existing pre-bond defects after bonding and to be able to add new post bond defects to the defect files. This involves flipping and combining the defect coordinate systems of the inverted wafers, and then combining all information into a new defect file appropriate for bonded wafers. The final goal was to add full automation with factory-host interface.

CSR: At this point in time, what is the status of the JDP?

GB: We've just installed the final version of the software in the tool at SEMATECH, and for all intents and purposes, the JDP is completed, with the final report under way. We actually went a bit beyond the scope of the project to provide some basic analysis tools for the overlay alignment data, including isolation and removal of various sources of error, along with graphical representation in the form of vector maps.

CSR: What would be a good application for this tool?

GB: Beyond inspection and metrology of bonded wafers and die, there are possibilities we'd like to explore in the back end, such as inspecting stacked die on tape to detect chip-outs and a possible 3rd optical inspection point. 3DIR could also be used to look for hotspots of 3D stacked ICs or packages during final test. There are some possibilities with SOI.

CSR: What is the technology roadmap going forward?

GB: We're working to add inspection capability - infrared scanning of wafers to detect voiding, thickness variations, and other defects. We believe we'll be able to offer advantages over current methods such as scanning acoustic microscopy (SAM). There are other possible modules to consider as well, and we would like to be able to offer our customers these modules as options on the same system in the future.